

디지털회로실험

월요일 057, 058 분반

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Orientation



디지털 회로 설계 실험

FPGA를 이용한

4비트 마이크로프로세서 설계 및 구현

박주성 · 최준영 공저



진샘미디어

- ✓ 실험 교재 : 디지털 회로 설계 실험 (진샘미디어)
- ✓ 실험 진행 중 휴대폰, 태블릿 사용 불가능 (e-book 불가능)
책 꼭 구매 후 실험 시간에 가지고 오세요
- ✓ 예비/결과 보고서는 수기로 작성 후 스캔하여 **PDF**로
매주 실험 전날 자정까지 실험도우미 메일로 제출
- ✓ 이후 제출시 감점 처리
- ✓ 실험 당일 검사도 있으니 예비/결과 보고서 지참해서 출석
(없으면 감점)
- ✓ 매 실험마다 교재, 예비 보고서, 결과 보고서 챙겨오기

Orientation

✓ 평가 방법 (각 분반별로 나눠서 학점 부여)

총 1000점

주별 과제물 (실험)	50%
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기말고사	20%
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예비/결과보고서	20%
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출석 및 태도	10%
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Orientation

구분	실험 내용	비고
1주	4 bit Processor 소개 및 Quartus 이용한 Half-adder, Full adder 설계	9/7
2주	Register 설계	9/14
3주	Encoder 설계	9/21
4주	Program Counter (PC) 설계	9/28
5주	Arithmetic Logic Unit (ALU) 설계	10/5
6주	Accumulator (ACC) 설계	10/12
7주	중간고사 휴강	10/19
8주	ALU & ACC 설계 #1	10/26

Orientation

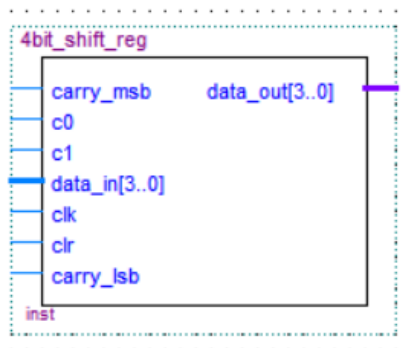
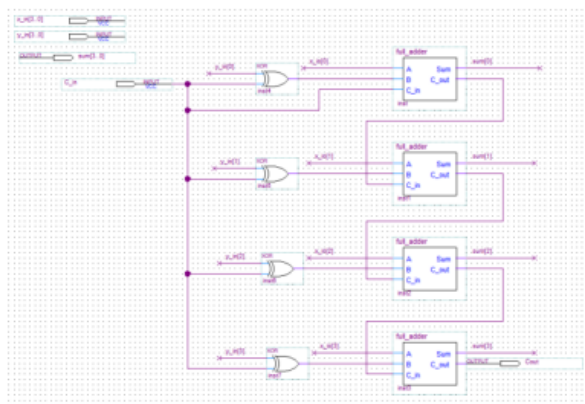
구분	실험 내용	비고
9주	ALU & ACC 설계 #2	11/2
10주	Control Block 설계 #1	11/9
11주	Control Block 설계 #2	11/16
12주	ROM & Hex to Decimal 설계	11/23
13주	Top Block 설계 #1	11/30
14주	Top Block 설계 #2	12/7
15주	기말고사 휴강 (Quiz)	미정

Orientation

- ✓ 실험 시간 휴대폰, 태블릿 사용 금지 부정행위로 간주 → 실험 0점 처리
실험에 필요한 내용은 예비 보고서에 작성
- ✓ 아래 행위들은 부정행위로 간주 → 이전 실험 전체 0점 처리
 - 1. 컴퓨터에 외부 장치(USB 등) 연결 금지 (휴대폰 충전도 불가능)
 - 2. 타 분반 계정 로그인 금지
- ✓ 실험 후 정리정돈 확인 (개별좌석 정리, 컴퓨터 전원 off) – 태도 점수 반영
- ✓ 매 수업 출석 체크 예정 (18:40 이후 출석 시 지각 처리)
4회 이상 결석 시 학과 담당조교에게 보고, 6회 이상 결석은 F
- ✓ 실습실 개별 개방 불가
결석 시 개인별 추가 개방은 제공되지 않으며, 다음 실습일에 이전
실습을 병행(2개 동시 진행)해야 합니다.
- ✓ 본 실험 전에 미리 해당 주차 실험을 해보는 것을 추천합니다.
- ✓ Quartus/Modelsim 설치 방법은 학과홈페이지 – 자유게시판 공지사항 참고

Orientation

- ✓ 결과보고서 작성 (문항 – 공지사항 참고)
- ✓ 매 실험 후 Quartus(회로도), symbol, testbench, Modelsim(파형) 총 4가지
- ✓ 핸드폰으로 컴퓨터 화면 사진 찍기 (캡처 및 USB 사용 불가능)
- ✓ 사진 없으면 손으로 그려야 합니다



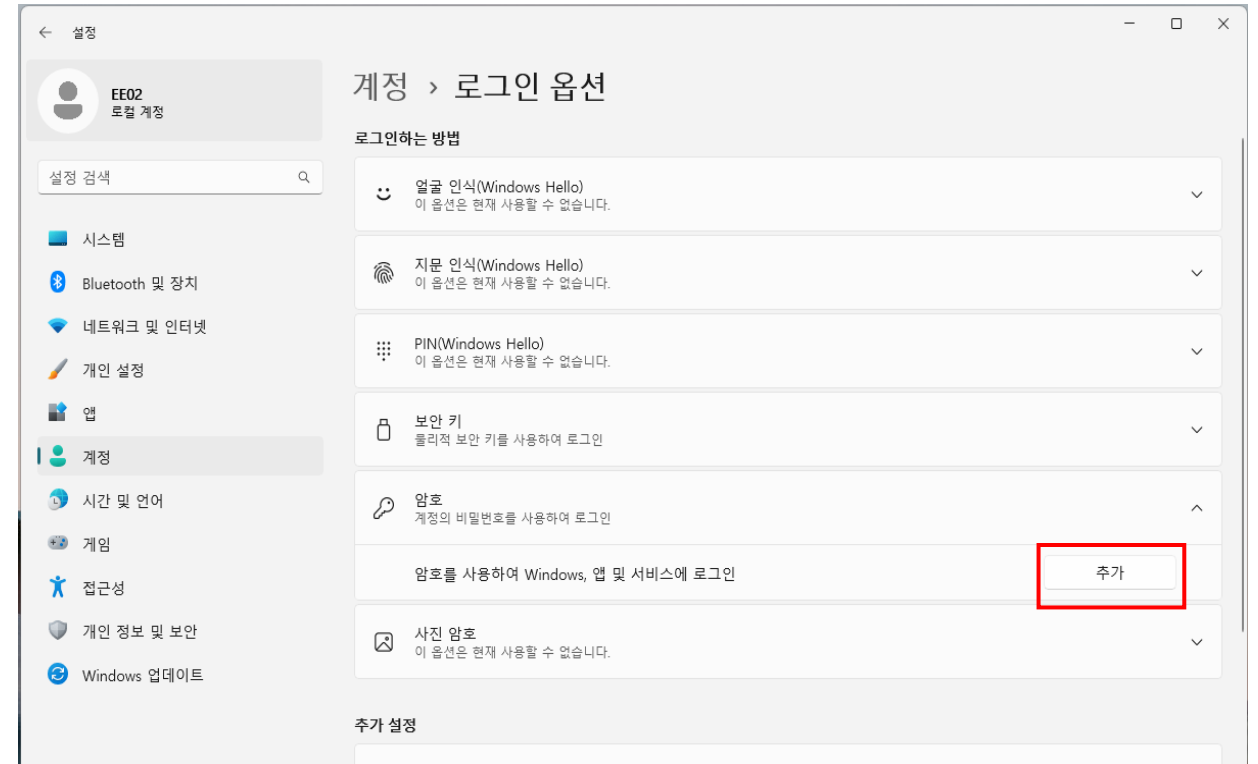
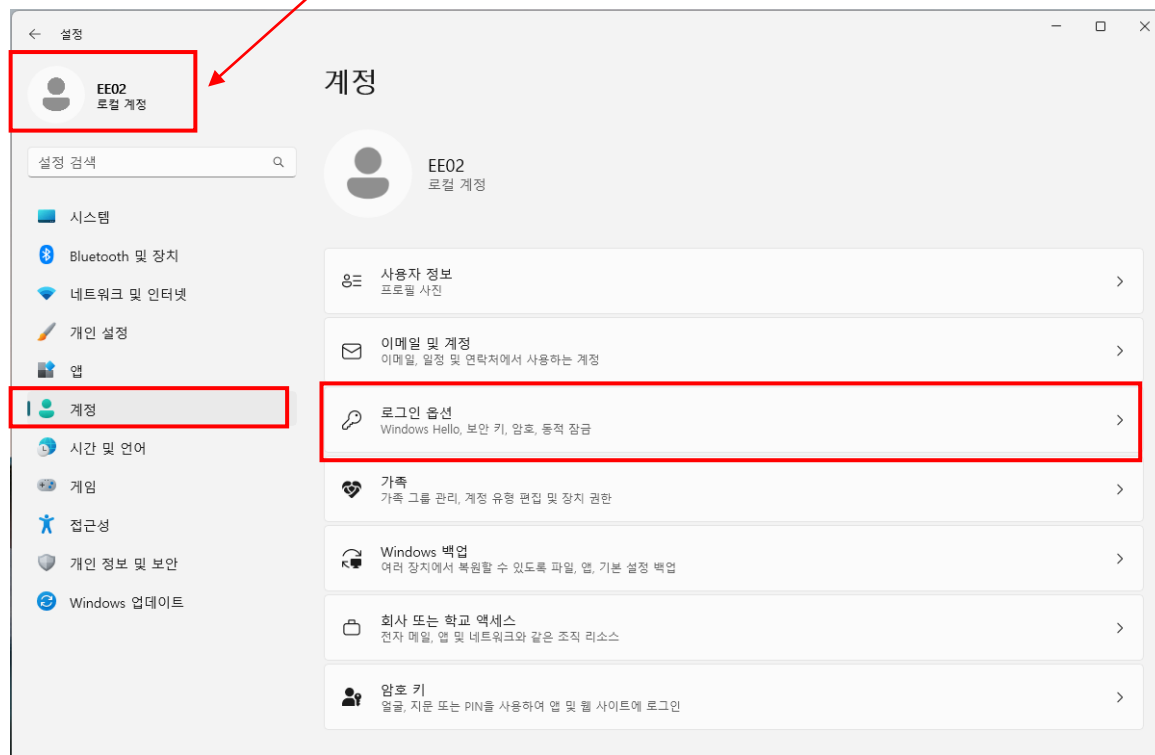
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1 module tb_ACC();
2
3 reg ah_reset;
4 reg clr;
5 reg clk;
6 reg ah_inen;
7 reg carry_out;
8 reg hsl;
9 reg hs0;
10 reg lsl;
11 reg ls0;
12 reg [3:0]ah_in;
13 reg [3:0]aludata;
14 wire [3:0]ah_out;
15 wire [3:0]al_out;
16
17 ACC uut(
18     .ah_reset(ah_reset),
19     .clr(clr),
20     .clk(clk),
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기말고사

- ✓ 실험 내용을 범위로 시험 진행
- ✓ 교재 및 예비/결과보고서 위주
- ✓ 일정: (추후 공지)
- ✓ 학과 강의실 진행 예정(추후 공지)

계정 비밀번호 설정

EE01 계정 확인!!



EE01 → 월요일 분반

EE02 → 화요일 분반

EE03 → 수요일 분반

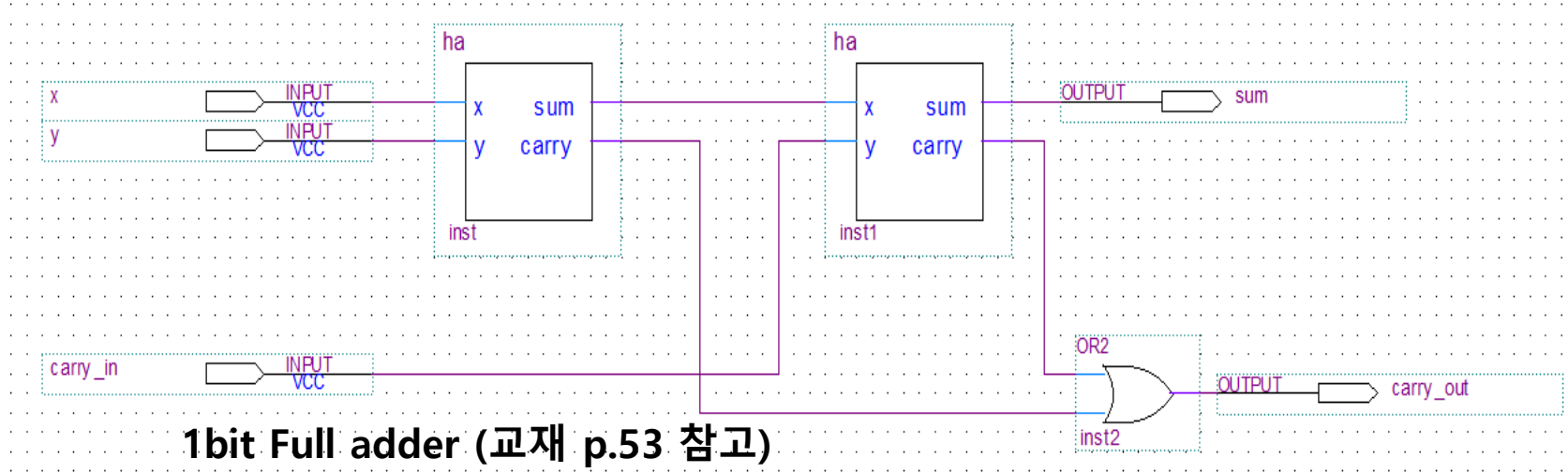
비밀번호 설정 필수

* 계정 공유 또는 비밀번호 유출 금지

- 부정행위 방지
- 개인 파일 보호

1주차 실험

1. Half adder 설계 및 시뮬레이션 (Modelsim 파형 검사)
 2. Full adder 설계 및 시뮬레이션 (Modelsim 파형 검사)
- 1번에서 설계한 Half adder를 심볼로 만들어서 사용

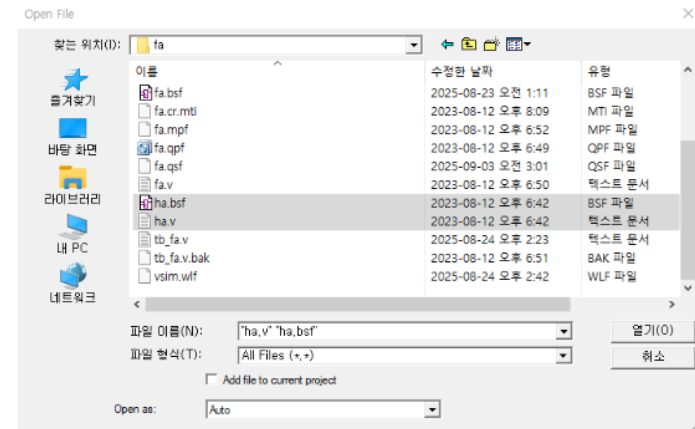
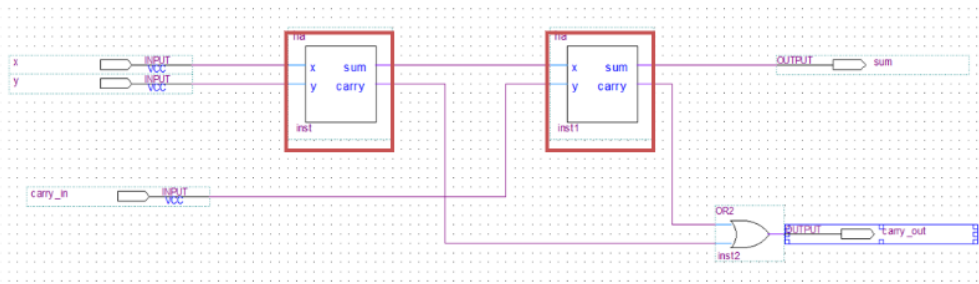


Full adder

X	Y	Cin	Sum	Cout
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1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

모든 경우에 대한 testbench
작성 후 Modelsim 파형 검사

- 검사: 종이에 좌석 번호 작성 후 대기 (검사 후 바로 퇴실!!!)
- 휴대폰, 태블릿 사용 및 외부 장치 연결 금지 (적발 시 이전 실험 전체 0점 처리)
- 교재, 예비/결과보고서 반드시 가져오기

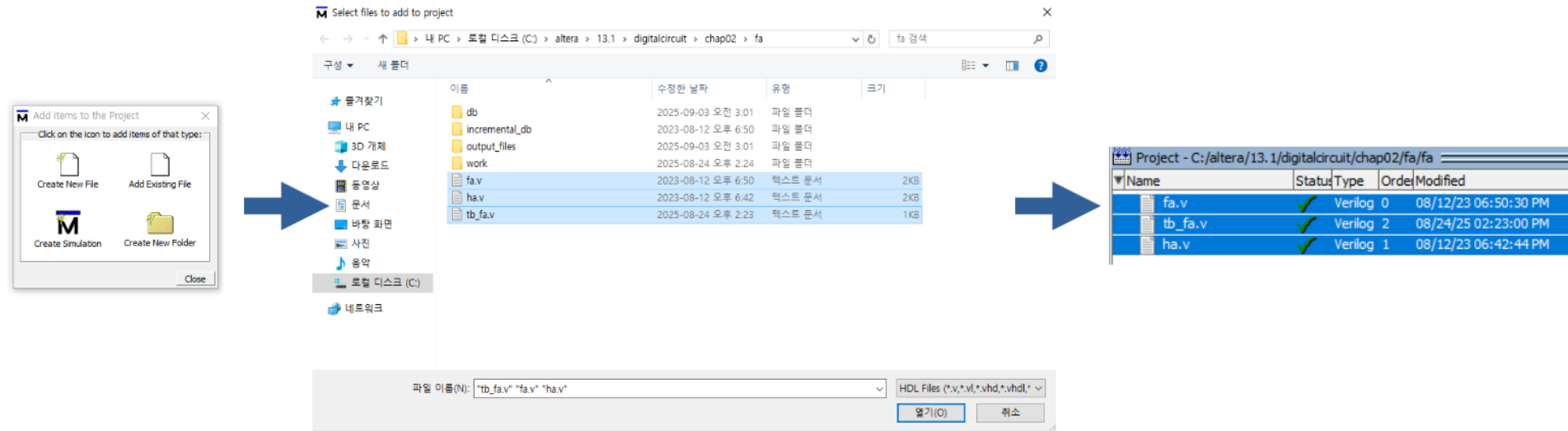


- ❌ 12006 Node instance "inst1" instantiates undefined entity "ha"
- ❌ 12006 Node instance "inst" instantiates undefined entity "ha"

● 다른 폴더 경로의 Quartus 프로젝트에서 생성한 심볼 파일(.bsf)을 사용했을 때 좌측 오류 발생 시, 해당 심볼의 원본 회로(위의 경우, ha)의 .v 파일(ha.v)과 .bsf 파일(ha.bsf)을 폴더에 추가

● Quartus - Project Wizard를 통해 Quartus 프로젝트 생성 시 파일 경로에 한글이 포함되지 않도록 해야하며, 바탕화면 경로는 한글로 취급됨에 유의

● Quartus 회로(.bdf) 및 테스트 벤치(tb_~.v) 파일 수정 후에는 반드시 컴파일 및 verilog HDL 파일(~.v) 생성 (재)진행하기



● 심볼 파일이 포함된 프로젝트의 ModelSim 프로젝트 생성 시, 위에서 추가해줬던 해당 심볼의 원본 .v 파일(위의 경우, ha.v)도 프로젝트에 추가

● ModelSim이 열려있는 상태로 Quartus 프로젝트 회로, 테스트 벤치 등 수정 후 컴파일해도, 수정사항이 자동 적용되지 않으므로 work 폴더 내 .v 파일들 update 및 recompile 필요

● ModelSim 결과 파형 중, 빨간 선은 테스트 벤치 등을 통해 초기 입력값을 설정해주지 않아 0, 1을 결정할 수 없음 / 파란 선은 회로 도선 끊김 또는 포트 비활성화 등으로 신호가 흐를 수 없음을 의미